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10/714,093	11/13/2003	Kevin D. Safford	200206543-1	9509

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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,093	SAFFORD ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-19 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on November 14th, 2003. The papers filed have been placed on record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 14, 15, 16, 17, 18, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Byrd (U.S. Publication No. 2002/1047044).

4. Regarding claim 14, Byrd discloses a method for selectively enabling an error detection mechanism comprising the steps of: a) maintaining a control register that includes an error detection enable bit; b) setting the error detection enable bit to enable the error detection mechanism; and c) clearing the error detection enable bit to disable the error detection mechanism (paragraph 55 last 5 lines).

5. Regarding claim 15, Byrd discloses the method of claim 14 wherein the step of setting the error detection enable bit to enable the error detection mechanism includes one of a user-programmed firmware setting the error detection enable bit to enable the error detection mechanism; an operating system setting the error detection enable bit to enable the error detection mechanism; and an application setting the error detection enable bit to enable the error detection mechanism (paragraph 55 last 4 lines);

Note that the "test software" is considered to be an application.

And wherein the step of clearing the error detection enable bit to disable the error detection mechanism includes one of a user-programmed firmware clearing the error detection enable bit to enable the error detection mechanism; an operating system setting clearing the error detection enable bit to enable the error detection mechanism; and an application clearing the error detection enable bit to enable the error detection mechanism (paragraph 55 last 4 lines).

6. Regarding claim 16, Byrd discloses the method of claim 14 wherein the error detection mechanism is enabled for a portion of critical code that includes a first instruction and a last instruction; wherein the step of setting the error detection enable bit to enable the error detection mechanism includes the step of setting the error detection enable bit to enable the error detection mechanism prior to the execution of the first instruction of the critical portion of code; and wherein clearing the error detection enable bit to disable the error detection mechanism includes clearing the error

detection enable bit to disable the error detection mechanism after the execution of the last instruction of the critical portion of code (paragraph 55 last 4 lines).

Note that the term "critical code" is being used out of a typical context, as understood by one of ordinary skill in the art. Typically, "critical code" or "critical section" is used regarding the acquisition of locks in a program. Due to this unusual environment for the term, Examiner viewed the specification and found no reasonable definition available for the term "critical code". So, for the purpose of this office action, critical code is considered to be, by definition, the code being executed while errors are enabled. So, the remaining limitations regarding critical code are both inherent by this definition and implied by the term in the last line of paragraph 55, "while testing the check bit generator", where said testing includes the critical code.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung (U.S. Patent No. 6,970,988) in view of Shoemaker (U.S. Publication No. 2003/0135711).

9. Regarding claims 1 ad 7, Chung discloses a processor that includes an execution) architecture for executing at least two instructions per cycle and at least two symmetric execution units (col 13 lines 30-33) comprising: a) instruction fetch unit for fetching n instructions (col 9 line 46); b) an instruction decoder for decoding the n instruction (col 9 line 47); wherein 2n instructions are processed per cycle (fig 14 and col 13 lines 37-38) c) duplication hardware for duplicating the n instructions into a first bundle and a second bundle (fig 14 and col 13 lines 33-38); wherein each bundle includes n instructions; d) a first execution unit for executing the first bundle of instructions in a first execution cycle (fig 14 reference 23-1); e) the second symmetric execution unit for executing the second bundle of instructions in the first execution cycle (fig 14 reference 23-2); f) comparison hardware for comparing the results of the first execution unit and the results of the second execution unit (fig 14 reference 58-12); and g) a commit unit for committing one of the results when the results are the same (col 13 lines 40-41); and h) an exception unit for generating an exception (raising a fault) when the results are not the same (col 13 lines 41-42).

Chung fails to distinguish whether or not the invention is an in-order or out-of-order processor.

Shoemaker discloses the use of an in-order processor (paragraph 21 line 2)

According to Shoemaker paragraph 21 lines 3-8, "the Pentium Pro, which is an out of order machine, uses about six and a half million transistors, requiring much more space than the in-order Pentium. Because of the additional transistors, the Pentium Pro also requires more power and generates more heat." These setbacks are a clear motivation to create an in-order machine.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Chung and allow it to be executed with in-order capabilities, as in Shoemaker.

10. Regarding claims 2 and 8, Chung/Shoemaker discloses the processor of claim 1 wherein the first execution unit issues the first bundle of instructions to the first execution unit; and wherein the second symmetric execution unit issues the second bundle of instructions to the second execution unit in the first execution cycle (fig 14 references 29-0, 29-12, 23-1 and 23-2).

Note the arros showing the transfer of data from DMB 0 and DMB 12 to the execution units 23-1 and 23-2 simultaneously (or, rather, during the same execution cycle).

11. Regarding claims 3 and 9, Chung/Shoemaker discloses the processor of claim 2 wherein the first execution unit is one of floating point unit, an integer unit, a arithmetic logic unit (ALU) (col 13 lines 29-30),

Note that the instruction being executed is an arithmetic instruction.

A multimedia unit, and a branch unit; and wherein the second execution unit is symmetric with respect to the first execution unit and includes one of floating point unit, an integer unit, a arithmetic logic unit (ALU) (col 13 lines 31-33), a multimedia unit, and a branch unit.

12. Regarding claims 4 and 10, Chung/Shoemaker discloses the processor of claim 1 wherein duplication hardware is provided for performing the instruction duplication and comparison hardware is provided for performing the comparison (fig 14 references 58-12 and 58-34),

Note in figure 14 the arrow from DMB0 and DMB12 splitting before entering execution units 23-1 and 23-2. This suggests the use of duplication hardware.

The method further comprising the step of: setting a bit in a control register; wherein the bit enables the duplication hardware and comparison hardware (col 13 lines 29-30).

Note the use of the term "redundancy mode". The term "mode" (in addition to other arithmetic examples in the reference) suggests that redundancy does not always occur. In order for this mode to be sometimes activated and sometimes not, there must be at least one bit that helps make this determination. The location of this bit is considered to be a "control register".

13. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung/Shoemaker in view of Byrd (U.S. Publication No. 2002/0157044).

14. Regarding claim 5, Chung discloses the processor of claim 4.

Chung fails to disclose the particular mechanism that toggles the redundancy mode (in other words, setting the bit associated to redundancy mode).

Byrd discloses an error detection bit (paragraph 55 last 3 lines) using an application/software (paragraph 55 4th to last line).

It is expected that one of ordinary skill in the art would appreciate the motivation for allowing a computer software application set and clear a bit that toggles an error detection mechanism. Applicant asserts that ultimately, no one understands the particular application being run on a particular processor as well as the person programmer. It is only logical to allow the programmer to have the ability to directly toggle a error detection mode using software code in order to optimize the application itself.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Chung and allow an application to toggle the redundancy (error detection) mode, as in Byrd.

Claims 6 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Chung/Shoemaker in view of Nishimoto (U.S. Patent No. 6,760,832).

15. Regarding claim 6, Chung discloses the processor of claim 1.

Chung fails to disclose a processor where n is equal to 3, suggesting that 6 instructions (three unique instructions, doubled) are processed per clock cycle. Instead, Chung discloses a processor where n is equal to 2.

Nishimoto discloses a technique of increasing the number of execution units (col 1 lines 54-58) to at least three (fig 1 reference 120).

In the environment of the primary reference, Chung discloses four execution units. Based on the motivation described in col 1 lines 54-58, Chung would be inclined to increase the number of execution units to six, meaning that n is equal to 3. The motivation stated in Chung is as follows, "In order to meet a growing demand for increasing operating speed, there has recently employed a method of increasing the number of arithmetic units to be simultaneously operated".

It would have been obvious at the time of the invention to allow the computing system of Chung to increase the number of execution units to six, as disclosed by Nishimoto.

16. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrd in view of Chung.

17. Regarding claim 17, Byrd discloses an apparatus for executing instructions comprising: a) a control register that includes an error detection enable bit (paragraph 55 last 3 lines); b) an error detection mechanism for detecting errors; and c) a mechanism for selectively enabling the error detection mechanism by setting the error

detection enable bit to enable the error detection mechanism and by clearing the error detection enable bit to disable the error detection mechanism (paragraph 55 last 4 lines).

Byrd fails to disclose if the error detection mode described is used for soft errors, as defined by Applicant to "cause an arbitrary node within the device to change state".

Chung describes a redundancy error-checking mode used to detect soft errors (col 13 lines 29-33).

Examiner asserts that the use of redundancy checking is becoming more common as processor components become smaller to avoid soft errors. It is clear why one of reasonable skill in the art would be motivated to utilize this mechanism. Furthermore, Byrd, who has the capability to toggle an error mode using an application, would be motivated to utilize this mechanism with the invention of Chung to give the programmer the ability to switch between a redundancy mode in the best interest of the application.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the system of Byrd and allow it to utilize the redundancy capabilities of Chung in such a way that the redundancy mode, as described by Chung, can be toggled using the mechanism of Byrd.

18. Regarding claim 18, Byrd/Chung discloses the apparatus of claim 17 wherein the selective enabling mechanism is one of a user-programmed firmware, an operating system, and an application (paragraph 55 4th to last line).

19. Regarding claim 19, Byrd/Chung discloses the apparatus of claim 17 wherein the error detection mechanism is enabled for a portion of critical code that includes a first instruction and a last instruction; wherein the selective enabling mechanism sets the error detection enable bit to enable the error detection mechanism prior to the execution of the first instruction of the critical portion of code; and wherein the selective enabling mechanism clears the error detection enable bit to disable the error detection mechanism after the execution of the last instruction of the critical portion of code (paragraph 55 4th to last line--see claim 16).

Conclusion

20. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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